Claims

What is claimed is:

1   1.   A redundancy circuit for a memory array comprising:
2   a miscompare detector for comparing a current address to be
3   accessed with a memory defect address; said miscompare detector
4   providing an enable redundant wordline signal responsive to a match of the
5   compared addresses;
6   a deactivate driver circuit coupled to said miscompare detector for
7   disabling non-redundant wordlines responsive to said enable redundant
8   wordline signal; and
9   a redundant driver coupled to said miscompare detector for enabling
10   redundant wordlines responsive to said enable redundant wordline signal.

1   2.   A redundancy circuit for a memory array as recited in claim 1
2   includes a wordline select circuit coupled to said redundant driver for
3   selecting a redundant wordline responsive to said enable redundant wordline
4   signal.

1   3.   A redundancy circuit for a memory array as recited in claim 1
2   wherein said miscompare detector includes a plurality of compare field effect
3   transistors coupled between a common precharge node and a common
4   discharge node.

1   4.   A redundancy circuit for a memory array as recited in claim 3
2   wherein said miscompare detector includes a precharge circuit coupled
3   between a supply voltage and said common precharge node and a
4   discharge device coupled between said common discharge node and
5   ground.

1   5.   A redundancy circuit for a memory array as recited in claim 4
2   wherein one of said plurality of compare field effect transistors is activated,
3   said common precharge node is discharged to identify a miscompare of the
4   compared addresses and an access to a non-redundant wordline is allowed.

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1   6.   A redundancy circuit for a memory array as recited in claim 1

2   wherein said match of the compared addresses is identified by said plurality

3   of compare transistors being deactivated, said common precharge node is

4   maintained in a precharge state.

1   7.   A redundancy circuit for a memory array as recited in claim 1

2   includes for each redundant wordline a miscompare detector for a wordline

3   read address and a miscompare detector for a wordline write address.

1   8.   A redundancy circuit for a memory array as recited in claim 7

2   wherein said deactivate driver circuit receives a common precharge node

3   signal for each said read address miscompare detector and each said write

4   address miscompare detector.

1   9.   A redundancy circuit for a memory array as recited in claim 1

2   wherein said deactivate driver circuit generates a reset signal to deactivate a

3   non-redundant wordline decoder responsive to said enable redundant

4   wordline signal.

1   10.   A redundancy circuit for a memory array as recited in claim 1

2   wherein said deactivate driver circuit includes a two-high field effect

3   transistor stack coupled between a reset common node and ground.

1   11.   A redundancy circuit for a memory array as recited in claim 10

2   wherein said deactivate driver circuit couples said enable redundant wordline

3   signal to said two-high field effect transistor stack to discharge said reset

4   common node responsive to said match and generate a reset signal to

5   deactivate a non-redundant wordline decoder.

1   12.   A redundancy circuit for a memory array as recited in claim 10

2   wherein said deactivate driver circuit includes a keeper circuit coupled to

3   said reset common node.

1   13.   A redundancy circuit for a memory array as recited in claim 10
2 wherein said deactivate driver circuit includes a saver transistor coupled to
3 said reset common node; said saver transistor being constantly activated
4 and said saver transistor providing said reset common node in a precharged
5 state when said deactivate driver circuit is activated.

1   14.   A redundancy circuit for a memory array as recited in claim 1
2 wherein said redundant driver coupled to said miscompare detector for
3 enabling redundant wordlines responsive to said enable redundant wordline
4 signal includes a buffer circuit receiving said enable redundant wordline
5 signal and providing a buffered enable redundant wordline signal output.

1   15.   A redundancy circuit for a memory array as recited in claim 2
2 wherein said wordline select circuit coupled to said redundant driver for
3 selecting a redundant wordline responsive to said enable redundant wordline
4 signal includes a wordline select circuit for a wordline read address and a
5 wordline select circuit for a wordline write address; said wordline select
6 circuit for said wordline read address and said wordline select circuit for said
7 wordline write address coupled to said deactivate driver circuit.

1   16.   A redundancy circuit for a memory array as recited in claim 15
2 wherein said wordline select circuit for said wordline write address includes a
3 dynamic write node and said wordline select circuit for said wordline read
4 address includes a dynamic read node; said dynamic write node and said
5 dynamic read node being precharged responsive to a clock output signal
6 generated by said deactivate driver circuit.

1   17.   A redundancy circuit for a memory array as recited in claim 15
2 wherein said wordline select circuit for said wordline write address receives a
3 write clock signal and said enable redundant wordline signal and said
4 wordline select circuit for said wordline read address receives a read clock
5 signal and said enable redundant wordline signal.

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1   18.   A method for disabling non-redundant wordlines and for

2   enabling redundant wordlines using a redundancy circuit for a memory array

3   comprising the steps of:

4   comparing a current address to be accessed with a memory defect

5   address;

6   providing an enable redundant wordline signal responsive to a match

7   of the compared addresses;

8   responsive to said enable redundant wordline signal, generating a

9   reset signal for disabling non-redundant wordlines; and

10   responsive to said enable redundant wordline signal, activating a

11   redundant wordline for said memory defect address.

1   19.   A method for disabling non-redundant wordlines and for

2   enabling redundant wordlines as recited in claim 19 wherein said generated

3   reset signal deactivates a wordline decoder for the memory array.

1   20.   A method for disabling non-redundant wordlines and for

2   enabling redundant wordlines as recited in claim 19 includes the step

3   responsive to a miscompare of the compared addresses, of allowing a

4   normal access to a non-redundant wordline.